ABSTRACT OF THE DISCLOSURE

A semiconductor device includes memory cells each having an MISFET for memory selection formed on one major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of the MISFET for memory selection via a first metal layer and an upper electrode formed on the lower electrode via a capacitive insulating film. The lower electrode has a thickness of 30 nm or greater at the bottom portion thereof. Sputtering with a high ionization ratio and high directivity, such as PCM, is adapted to the formation of the lower electrode to make only the bottom portion of a capacitor thicker.